

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electrical impedance tomography (EIT) data processing system, for acquiring and processing data from two-phase flows, comprising a dual-plane sensor, a plurality of digital signal processing modules configured in a data pipeline processing arrangement and a plurality of data acquisition subsystems in communication with a first one of said plurality of digital signal processing modules; wherein at least one of the data acquisition subsystems includes an over-zero switch comprising: at least one multiplexer and at least one flip-flop; the at least one multiplexer and at least one flip-flop; the at least one multiplexer arranged to supply a sinusoidal signal to a selected one of a plurality of channels of the dual-plane sensor according to an output of the at least one flip-flop; the at least one flip-flop arranged to receive a synchronization signal that has the same over-zero point as the sinusoidal signal, the synchronisation signal causing the at least one flip-flop to output a channel selection signal provided to the at least one flip-flop to output a channel selection signal provided to the at least one flip-flop.
2. (Currently Amended) ~~A-~~ The system as claimed in claim 1 wherein said data acquisition subsystems are in communication with a first one of said plurality of digital signal processing modules via a data acquisition interface.
3. (Currently Amended) ~~A-~~ The system as claimed in claim 1, wherein the data pipeline processing arrangement is capable of acquiring and/or processing 1000 dual frames per second per dual-plane.
4. (Currently Amended) ~~A-~~ The system as claimed in claim 1, wherein said digital signal processing modules are selectively in communication with a remote PC, ~~preferably via an~~ IEEE1394 interface.

5. (Currently Amended) ~~A- The~~ system as claimed in claim 1, wherein a first one of said digital signal processing modules is capable of controlling data acquisition and processing.
6. (Currently Amended) ~~A- The~~ system as claimed in claim 1, wherein a second one of said plurality of digital signal processing modules is capable of image reconstruction.
7. (Currently Amended) ~~A- The~~ system as claimed in claim 1, wherein the plurality of digital signal processing modules comprises four digital processing modules and wherein a third one of said plurality of digital signal processing modules is capable of performing velocity calculations by fusing image data to obtain flow information.
8. (Currently Amended) ~~A- The~~ system as claimed in claim ~~4~~ 7, wherein a fourth one of said ~~plurality of~~ digital signal processing modules is capable of being configured to carry out additional selected functions.
9. (Currently Amended) ~~A- The~~ system as claimed in claim 1, further comprising transducers for obtaining conductivity, pressure and/or temperature information, the transducers being in communication with one of said data acquisition subsystems.
10. (Currently Amended) ~~A- The~~ system as claimed in claim 1, wherein said dual-plane sensor comprises an electrode array in communication with one of said data acquisition subsystems.
11. (Currently Amended) ~~A- The~~ system as claimed in claim 1, wherein said data acquisition subsystems each include ~~one or more of~~ a voltage controlled current source, an equal-width pulse synthesiser, and a synchronised digital demodulation unit ~~and an over-zero switch~~.
12. (Currently Amended) ~~A- The~~ system as claimed in claim 11, wherein said voltage controlled current source comprises a parallel structure of eight AD844 chips ~~or equivalents~~, configured as four pairs in which the two inverting inputs of each pair are ~~each~~ connected together with a current-setting resistor.

13. (Currently Amended) ~~A-~~ The system as claimed in claim 12, wherein the four negative current outputs of the four pairs of AD844 chips are summed together to provide a total negative current output.

14. (Currently Amended) ~~A-~~ The system as claimed in claim 12, wherein the four positive current outputs of the four pairs of AD844 chips are summed together to provide a total positive current output.

15. (Currently Amended) ~~A-~~ The system as claimed in claim 12, wherein the voltage controlled current source further comprises a DC restore facility in which a capacitor and a resistor connected to ~~the~~ a non-inverting input of each AD844 an OPA602 chip, wherein the capacitor is connected to an output of the OPA602 chip and the resistor is connected to an output of a first AD844 chip of the parallel structure, restores DC components generated in the system and cancels ~~the~~ a DC offset at the negative and positive current outputs of the AD844 chips.

16. (Currently Amended) ~~A-~~ The system as claimed in claim 12, wherein the voltage controlled current source includes a potentiometer for amplitude balancing.

17. (Currently Amended) ~~A-~~ The system as claimed in claim 11, wherein said equal-width pulse synthesiser comprises a clock signal for triggering an address generator to continuously output addresses to a pre-programmed memory, the memory output being connected to a digital to analogue converter, the digital to analogue converter providing a staircase signal output, ~~characterised in that~~ wherein the equal-width pulse synthesiser has different sampling rates ~~are provided~~ at different signal frequencies so that the staircase signal output has the same time step-length at all frequencies.

18. (Currently Amended) ~~A-~~ The system as claimed in claim 17 wherein said equal-width pulse synthesiser further comprises a low pass filter connected to the output of the digital to analogue converter to provide a smoothed signal output.

19. (Currently Amended) ~~A- The~~ A system as claimed in claim 11, wherein said synchronised digital demodulation unit comprises 16 ~~sets of~~ programmable gain amplifiers each having an analogue to digital converter, ~~a two~~ strobed First-In First-Out (FIFO) memory ~~memories~~ and control logic.
20. (Currently Amended) ~~A- The~~ system as claimed in claim 19, wherein the signal output of the equal-width pulse synthesiser triggers said 16 analogue to digital converters to acquire measurement data in parallel at predefined intervals.
21. (Currently Amended) ~~A- The~~ system as claimed in claim 11, wherein said over-zero switch comprises two multiplexers, each having 16 electrodes mounted in one sensing plane connected to their 16 output channels and two flip-flops controlled by a switching command from one of said DSP modules.
22. (Currently Amended) ~~A- The~~ system as claimed in claim ~~21~~, 1 wherein said over-zero switch further comprises a D-type flip-flop ~~for preventing data being written prematurely to the second of said flip-flops.~~
23. (Cancelled)
24. (Currently Amended) A method of processing electrical impedance tomography comprising:  
a) providing a system as claimed in claim 1; and  
b) processing electrical impedance tomography data ~~from two phase flows~~ for a two phase flow.
25. (Cancelled)
26. (Currently Amended) A non-transitory recording medium having recorded thereon computer implementable instructions for performing the method of claim 24 or claim 25.